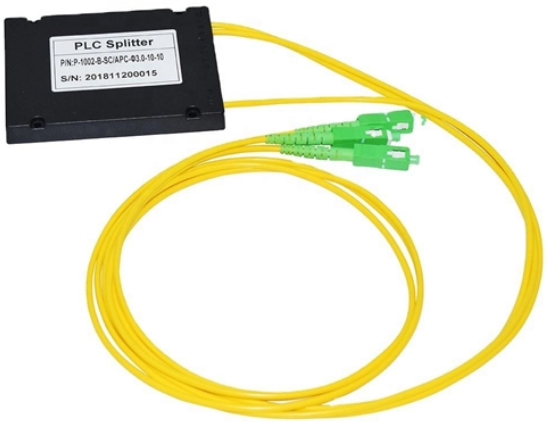
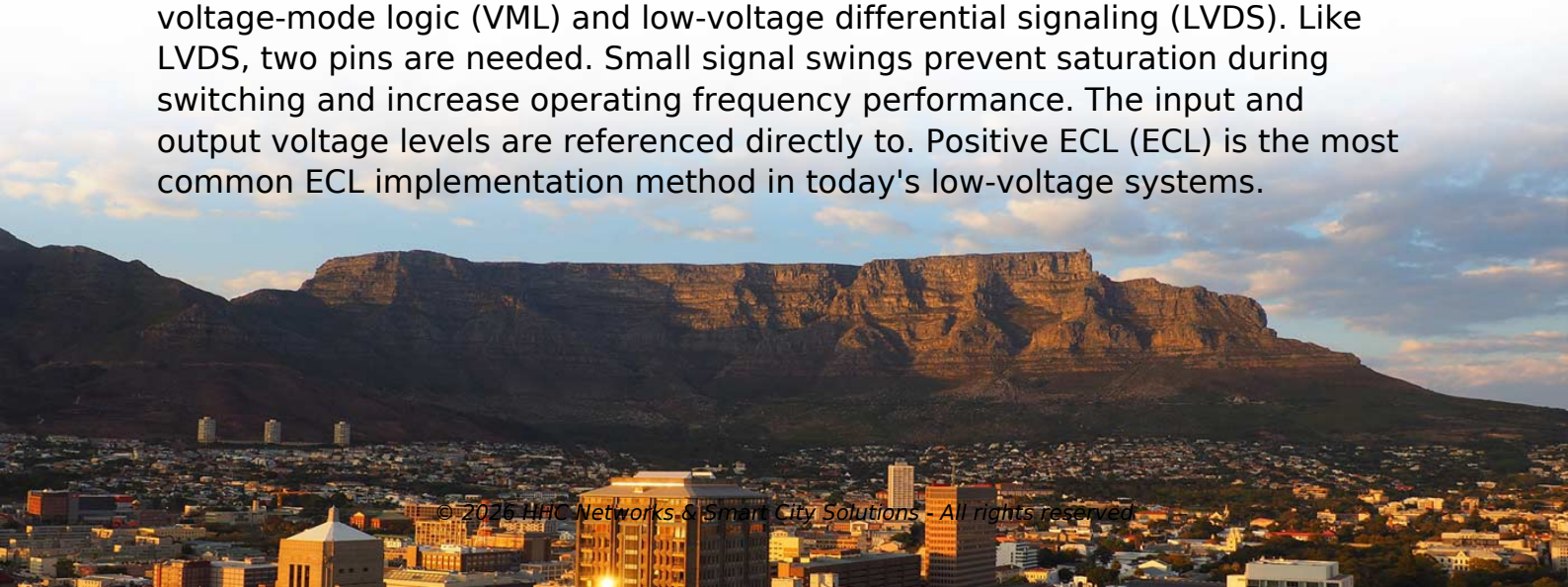
LVPECL level of optical module

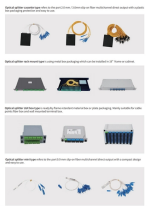


Overview

The correct level for DC-coupled applications is VCC–2V. Many of Micrel's devices include a VBB reference voltage pin; proper set-up is shown in Figure 6. LVPECL is an established high frequency differential signaling standard that requires external passive components for proper operation. For DC coupled logic, these external components bias both the LVPECL driver into conduction and terminate the associated differential transmission line. However. The main logic levels discussed in this application report are low-voltage positive/pseudo emitter-coupled logic (LVPECL), current-mode logic (CML), voltage-mode logic (VML) and low-voltage differential signaling (LVDS). Like LVDS, two pins are needed. Small signal swings prevent saturation during switching and increase operating frequency performance. The input and output voltage levels are referenced directly to. Positive ECL (ECL) is the most common ECL implementation method in today's low-voltage systems.



LVPECL level of optical module

	If an application requires interfacing from LVDS to LVPECL, direct interface is possible provided the LVPECL line receiver has the proper differential common mode input range.
	Split Supply Termination (LVPECL) Although rarely used in end applications, split power supply termination is often used to take advantage of the internal 50 Ohms termination of an oscilloscope or ...
	The MC100LVEL92 is a triple PECL input to LVPECL output translator. The device receives standard PECL signals and translates them to differential LVPECL output signals.
	LVPECL is derived from ECL and PECL and typically uses 3.3 V and ground supply voltage.
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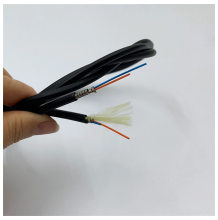

There are many different termination schemes for the LVPECL drivers; this application note covers the standard DC coupled terminations as well as biasing LVPECL drivers for AC coupling.

To accomplish LVPECL to LVDS interfacing the proposal scheme uses the Thevenin Equation to fix the static level of the LVDS input. The LVPECL differential output swing will surely go over the LVDS ...

LVPECL and PECL are both offshoots of the older ECL technology, first introduced in the 1960s. PECL stands for Positive Emitter Coupled Logic as it operates off a positive voltage such as 5V, 3.3V, or 2.5V.

The LVPECL circuit is similar to the LVDS scheme. It requires four external resistors, three for the driver and one for the receiver. The values for the three driver resistors are different from that of LVDS ...

When included in a comparison between LVDS and LVPECL, LVDS provides more channels (16 versus 10) and requires less power than LVPECL when operating over 50 to 600 Mbps (20 to 300MHz clocks).

PECL applies to 5V systems, while low-voltage PECL (LVPECL) applies to +2.5V and +3.3V systems. Micrel has an extensive logic and clock synthesis/generation family specified for PECL and LVPECL ...

Contact Us

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